**Lesson Plan**

**Name of faculty: SUNIL KUMAR DAHIYA, AP-ECE**

**Discipline: ECE**

**Semester: 3rd**

**Subject: Digital Electronics (ECE-207N) and Digital Electronics lab(ECE-213N),**

Lesson Plan Duration: 15 weeks (from July, 2018 to Nov., 2018)

Work Load (Lecture/Practical/Tutorial) per week (in hours):

 **Lectures: 03 hours, Practical: 06hours and Tutorials: 02hours**

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| **+** | **Theory** | **Practical** |
|  | **Lecture day** | **Topic(Including assignment/ test)** | **Practical day** | **Topic** |
| 1st |  | Digital Systems | 1 | Study of TTL gates AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR. |
|  | Logic circuits, Analysis, design and implementation of digital systems |  |  |
|  | Number Systems and Codes-Positional number system; Binary |  |  |
| 2nd |  | Octal and Hexadecimal arithmetic; Representation of signed numbers; Fixed and floating point numbers | 2 | Design and realize a given function using K-Maps and verify its performance. |
|  | Binary codes: BCD codes, Excess-3, Gray codes, Error detection |  |  |
|  | Correction codes -parity check codes and Hamming code |  |  |
| 3rd |  | Combinational Logic Systems: Definition and specification | 3 | To verify the operation of Multiplexer and De-multiplexer. |
|  | Truth table; Basic logic operation and logic gates |  |  |
|  | Basic postulates and fundamental theorems of Boolean algebra |  |  |
| 4th |  | Standard representation of logic functions : SOP and POS forms | 4 | To verify the operation of 2 bit Comparator using gates |
|  | Simplification of switching functions using K-map  |  |  |
|  | Quine- Mc Cluskey tabular methods |  |  |
| 5th |  | Synthesis of combinational logic circuits using AOI, NAND,NOR |  |  |
|  | Other combination of other logic functions |  |  |
|  | Introduction to different logic families |  |  |
| 6th |  | Operational characteristics of BJT in saturation and cut-off regions | 5 | To verify the truth table of S-R, J-K, T, D Flip-flops. |
|  | Operational characteristics of MOSFET as switch |  |  |
|  | TTL inverter -circuit description and operation; CMOS inverter -circuit description and operation |  |  |
| 7th |  | Structure and operations of TTL ,CMOS and ECL gates | 6 | To verify the operation of Bi-directional shift register. |
|  | Electrical characteristics of logic gates –logic levels and noise margins |  |  |
|  | Fan-out, propagation delay, transition time |  |  |
| 8th |  | Power consumption and power-delay product; interfacing of TTL and CMOS families | 7 | To design and verify the operation of 3-bit asynchronous counter. |
|  | Encoders, Decoders, multiplexers, de-multiplexers and their use as logic elements |  |  |
|  | Parity circuits and comparators;  |  |  |
| 9th |  | Arithmetic modules-adders, subtractors , BCD arithmetic circuits |  |  |
|  | Definition of state machines, state machine as a sequential controller |  |  |
|  | Basic sequential circuits-latches and flip-flops |  |  |
| 10th |  | SR-latch, D-latch, D flip-flop | 8 | To design and verify the operation of asynchronous Up/down counter using J-K FFs. |
|  | JK flip-flop, T flip-flop |  |  |
|  | Timing hazards and races |  |  |
| 11th |  | Analysis of state machines using D flip-flops and JK flip-flops | 9 | Design a state machine of 4 states. |
|  | Design of state machines -state table, state assignment, transition/excitation table, excitation maps and equations, logic realization |  |  |
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| 12th |  | Designing state machine using ASM charts | 10 | To design a sequence detector. |
|  | Designing state machine using state diagram |  |  |
|  | Design of registers, counters-asynchronous and synchronous,  |  |  |
| 13th |  | up/down counter, Ring and Johnson counters |  |  |
|  | Definition of state machines |  |  |
|  | state machine as a sequential controller |  |  |
| 14th |  | Organization, Functional Diagram, Memory operations |  |  |
|  | Classification of semiconductor memories, Read and Write Memories, ROM |  |  |
|  | Programmable Logic Devices-PLAs |  |  |
| 15th |  | PALs and their applications |  |  |
|  | Generic Array logic devices, Sequential PLDs and their applications |  |  |
|  | Introduction to field programmable gate arrays (FPGAs) and ASIC. |  |  |